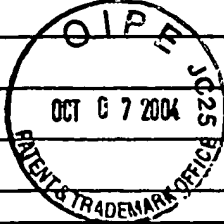


INFORMATION DISCLOSURE CITATION

Atty. Docket No.	2887.0269	Appln. No.	10/804,159
Applicant	Hieda et al.		
Filing Date	March 19, 2004	Group:	2811



U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
MH	2004/0072429 A1	4/15/04	Hieda et al.			

FOREIGN PATENT DOCUMENTS

	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
MH	2003-31650	1/31/03	Japan			Abstract
MH	2002-367980	12/20/02	Japan			Abstract

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MH	Sato et al., "Advanced Spin Coating Film Transfer and Hot-Pressing Process for Global Planarization with Dielectric-Material-Viscosity Control," Jpn. J. Appl. Phys. (April 2002), 41:2367-73

Examiner	<i>Michael...</i>	Date Considered	10/26/05
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INFORMATION DISCLOSURE CITATION

Atty. Docket No. 02887.0269	Application No.
Applicant Katsuhiko HIEDA et al.	
Filing Date March 19, 2004	Group: Not assigned

U.S. PATENT DOCUMENTS						
Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
<i>UH</i>	6,479,405 B2	11/12/02	Lee et al.			
<i>UH</i>	2003/0022522 A1	1/30/03	Nishiyama et al.			

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	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
<i>UH</i>	2000-114362	4/21/00	Japan			Abstract
<i>UH</i>	2000-183150	6/30/00	Japan			Abstract
<i>UH</i>	2001-308090	11/2/01	Japan			Abstract
<i>UH</i>	2002-203895	7/19/02	Japan			Abstract

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<i>UH</i>	Jin-Hwa Heo et al., "Void Free and Low Stree Shallow Trench Isolation Technology using P-SOG for sub 0.1 μ m Device". Symposium On VLSI Technology Digest of Technical Papers. pp. 132-133 (2002)
<i>UH</i>	Yukio NISHIYAMA et al., "Method for Manufacturing Semiconductor Device", U.S.Serial No. 10/193,143, filed July 12, 2002.

Examiner <i>M. Schubert</i>	Date Considered <i>10/26/05</i>
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